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A HIGH PERFORMANCE, QUASI-MONOLITHIC 2 TO 18 GHz DISTRIBUTED GaAs FET AMPLIFIER

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ABSTRACT

Design, fabrication, and performance of a quasi-monolithic distributed GaAs FET amplifier is discussed. A gain of 20 dB and noise figure of 5.8 dB over 2 to 18 GHz are achieved. The amplifier circuits, using modified commercially available GaAs FET chips, are ideal for moderate volume (less than 5000), high performance applications.

INTRODUCTION

This paper describes the design, fabrication and performance of a quasi-monolithic distributed GaAs FET amplifier with 20-dB gain and a noise figure of 5.8 dB maximum over the 2 to 18 GHz frequency band. The GaAs FET's are commercially available chips that have been modified, attached with epoxy and wire-bonded to the monolithic amplifier circuit which is fabricated on a semi-insulating GaAs substrate.

The quasi-monolithic approach has been described in detail.(1) In short, quasi-monolithics combine the size and batch-processing advantages of monolithics with the superior performance and yield achievable with discrete devices. They are comparable in size to monolithic circuits and utilize the same processing techniques to fabricate air bridges, overlay capacitors and via holes. The lowest yield to date for the circuits prior to FET attachment is 70 percent.

For moderate-volume (less than 5000 chips), high-performance applications where monolithic may not be cost-effective, quasi-monolithic can be an affordable technology. The excellent performance achievable with quasi-monolithic technology is evident in the noise figure measured for this unit which is believed to be the lowest ever reported for a 2 to 18 GHz distributed amplifier.

DESIGN

The theory of distributed amplifiers was originally proposed by Ginzton, et al(2). Its recent resurgence as a technique for broadband microwave amplification has been thoroughly covered in several recent papers(3,4,5) and will not be covered in this work. The basic disributed amplifier schematic is shown in Figure 1. In general, a very low gate capacitance is required to place the cutoff frequency of the loaded gate transmission line above the desired frequency of operation.

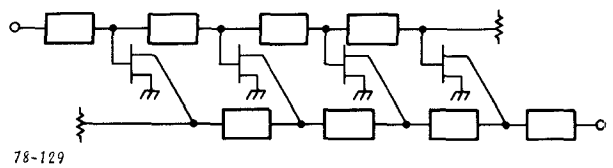

Figure 1. General Distributed Amplifier Schematic

To achieve the required gate capacitance a modified GaAs FET chip was used. The device is normally a two-cell FET with a total gate periphery of 300 microns. The chip was cut in half with a dicing saw, effectively reducing the periphery to 150 microns (and the capacitance by a factor of two) by using only one of the two available cells. After measuring and de-embedding the device S-parameters, a model was developed for the device (Figure 2). Gate and drain port models were extracted from this model. The equivalent electrical models for the amplifier input and output circuits are shown in Figures 3a and 3b, respectively.

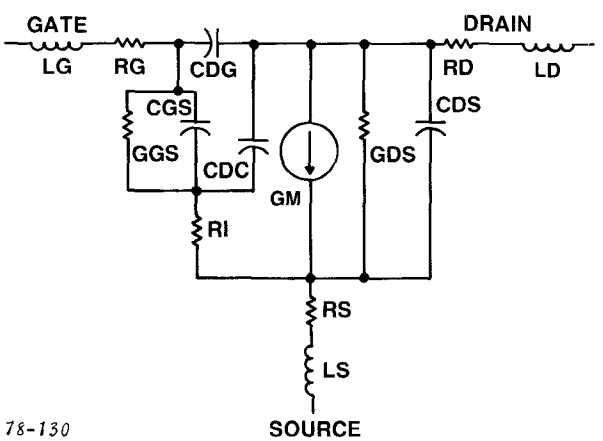

Figure 2. GaAs FET Model

The circuit and transistor models were combined and the resultant amplifier circuit was analyzed using a microwave computer-aided analysis program. The circuit values were optimized for flat gain and minimum VSWR over the band. The predicted noise figure was calculated using the technique described by Colin S. Aitchinson(6). A critical portion of the amplifier is the bias-

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injection circuit. This circuit must provide high isolation between the dc input to the amplifier and the drain transmission line where bias is distributd to the four FET's. Bias current cannot be injected through the drain terminating resistor because the high dissipated power would far exceed the power capability of the small thin-film resistor.

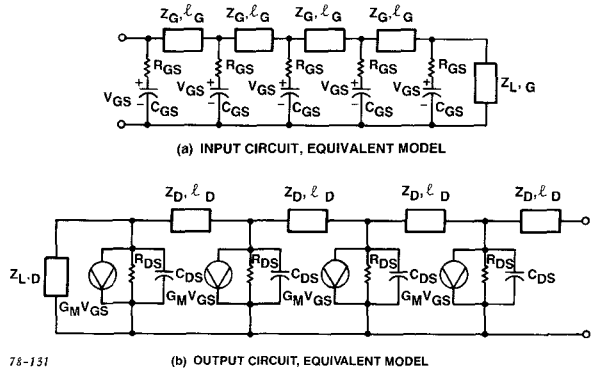

Figure 3. Distributed Amplifier Equivalent Input and Output Circuits

The final circuit schematic is shown in Figure 4 and the predicted gain for the single stage is shown in Figure 5.

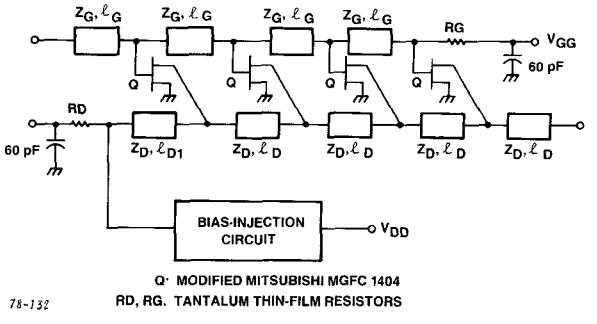

Figure 4. Single-Stage Distributed Amplifier Schematic

CIRCUIT FABRICATION

The quasi-monolithic distributed 2 to 18 GHz amplifier chip is fabricated using sputtered tantalum and gold metallurgy. All of the metal layers are deposited in-situ upon a GaAs Semi-Insulating substrate in a Perkin Elmer Sputter system. The in-situ method of depositing all of the metals and Ta_2O_5 consecutively results in a substantial increase in capacitor reliability and yield. Less than 1 percent of capacitors exhibit failures due to pin holes and greater than 95 percent of capacitors are accepted after testing. The overall chip yield after dicing was 70 percent. The chip yield is significantly better than for monolithic circuits.

Figure 6 shows a diagram of all the metal and oxide layers after deposition as well as the subsequent definition of these metal layers via dry etching techniques. After these layers are etched, via holes and air bridges are defined.

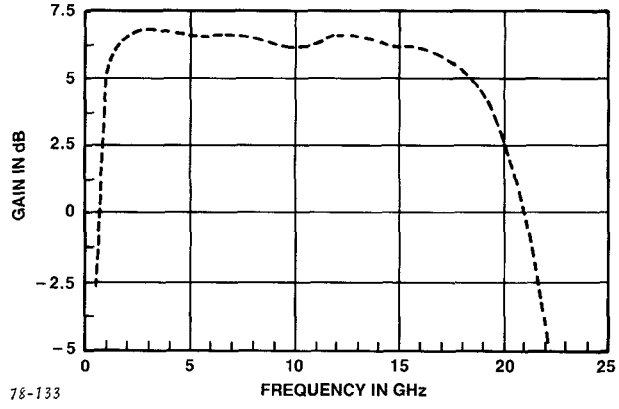

Figure 5. Predicted Single-Stage Gain

After the passive circuit chips are fabricated and diced, they are attached to carriers with conductive silver epoxy. The modified FET devices are attached to the amplifier chip with conductive epoxy and bonded to the circuit using 0.7-mil diameter gold wires.

MEASURED RESULTS

A single stage, four-cell amplifier, shown schematically in Figure 4, was fabricated, assembled, and tested. A photograph of this circuit is shown in Figure 7. Based on the excellent results of the single-stage measurements, a three-stage amplifier was assembled by directly cascading three chips in a common fixture.

The gain of the three-stage amplifier is nominally 22 dB with about 6 dB variation across the band. The noise figure varies from 5.8 dB at the band edges to 4.8 dB at 11 GHz. This is believed to be the lowest noise figure reported for MMIC distributed amplifier in this frequency range. The gain and noise figure are shown in Figures 8 and 9, respectively. The input and output return losses plotted in Figure 10 are generally better than 10 dB except at the upper band edge where they degrade sharply. Some of this may be due to a connector interfacing problem. The measured third-order intercept point is greater than 20 dBm except at one point in the band where it drops to 19 dBm.

It should be noted that with selection of higher I_{DSS} devices and an output stage I_{DS} of 90 mA, third-order intercept points of 25 dBm are possible. This was verified during testing of the single-stage amplifier when intercept points of 25, 40, and 46 dBm were measured for third order, second order and second harmonic products, respectively.

The total direct current power required for the three-stage amplifier is approximately 500 mW. The area occupied by three-amplifier chips is approximately 20 mm^2. Table 1 lists the results of the initial tests on the amplifier.

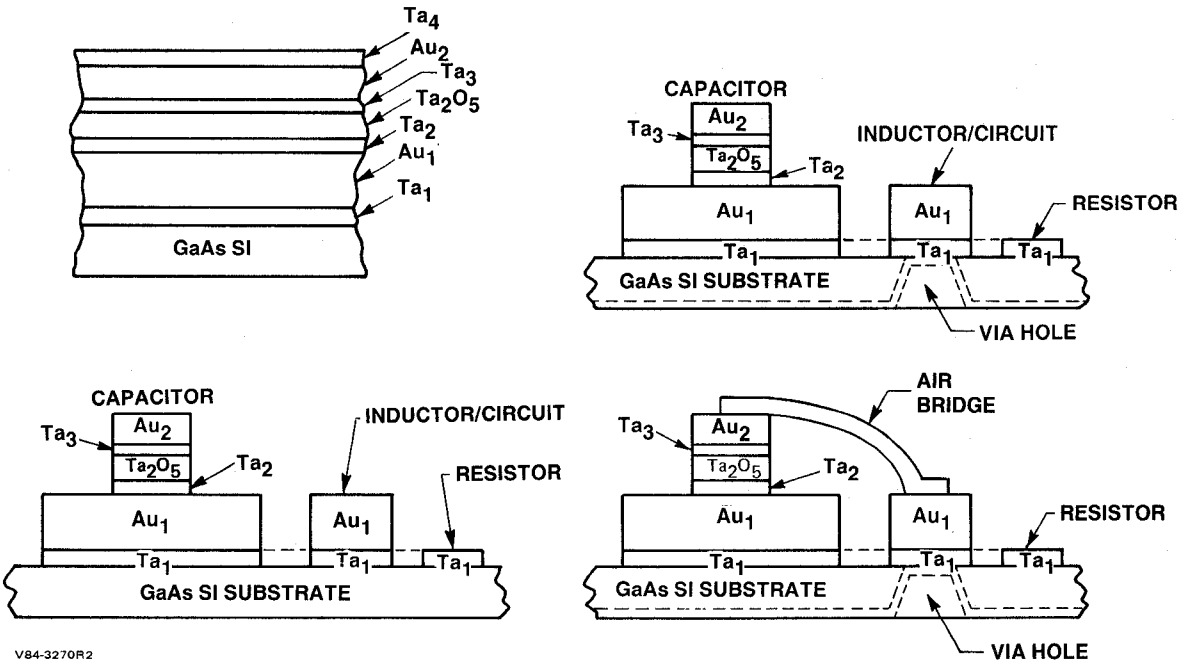

Figure 6. Process Steps to Define Monolithic Passive Elements

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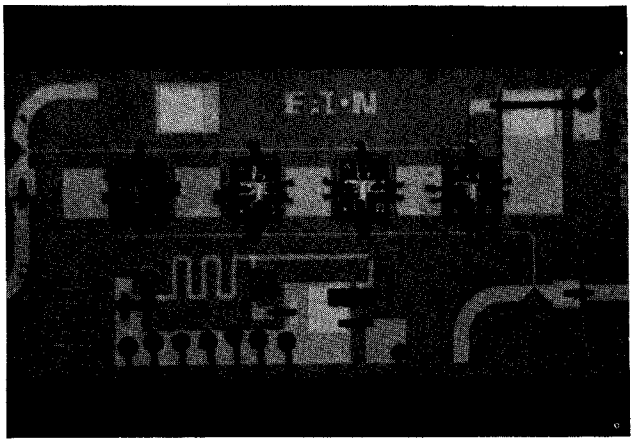

Figure 7. Amplifier in Test Fixture

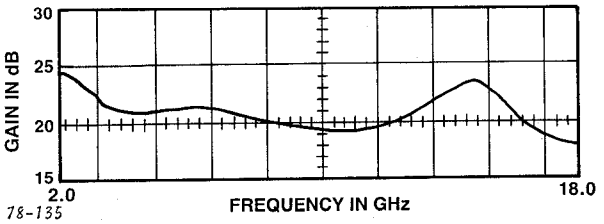

Figure 8. Three-Stage Distributed Amplifier Measured Gain

Table 1. Three-Stage Q-M Distributed Amplifier Preliminary Measured Results

Frequency	2 to 18 GHz
Gain	18 to 24 dB
Noise Figure	5.8 dB max
VSWR, Input	1.6:1 2 to 16 GHz 2.0:1 16 to 18 GHz
VSWR, Output	2.5:1 2 to 16 GHz 3.0:1 16 to 18 GHz
IP3	19 dBm min*
IP2	29 dBm min*
IPH2	35 dBm min*
Reverse Isolation	50 dB min
Dc Power	+5V, 140 mA -3V, 10 mA
Size	1.7 mm x 11.4 mm

* Can be improved with higher I_{DSS} device selection.

CONCLUSION

A distributed amplifier with 20-dB gain and noise figure of 5.8 dB maximum over the 2 to 18 GHz band has been demonstrated. This performance was achieved using a quasi-monolithic technique which combines a monolithic passive circuit and discrete FET's.

The technology is affordable for moderate quantities in view of the excellent chip yields of at least 70 percent.

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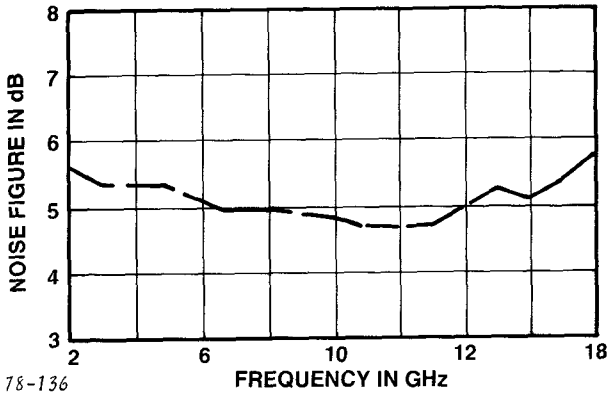

Figure 9. Measured Noise Figure

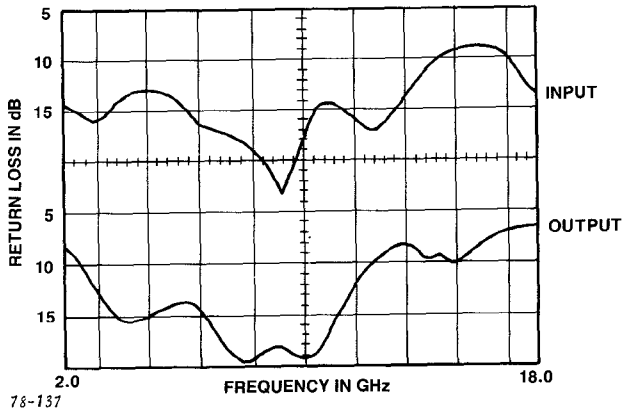

Figure 10. Measured Input and Output Return Loss

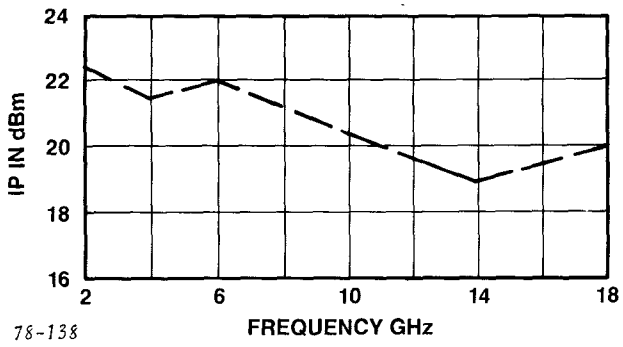

Figure 11. Measured Third-Order Intercept Points

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